ENROO 英锐恩 *单片机集成方案全方位解决服务商*

优质智能电子产品“芯”方案解决商

深圳市英锐恩科技有限公司

EN1621 LCD 驱动芯片

Add:深圳市福田区福华路嘉汇新城汇商中心 2701 **http://www.enroo-Tech.com**
Tel:+86-0755-82543411, Fax: +86-0755-82543511 http://www.enroo.com
企业热线 4007-888-234

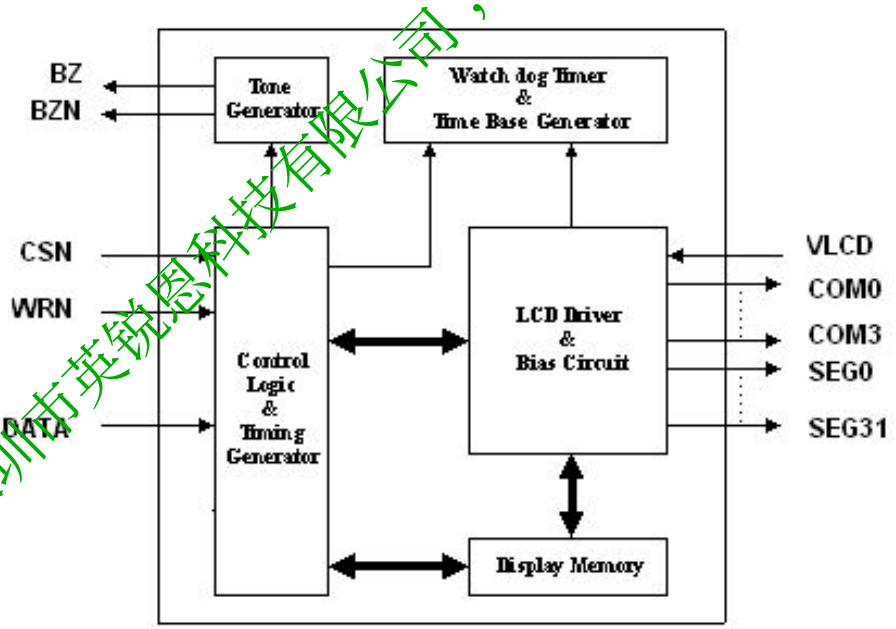
General Description

The EN1621 is a 128 dots (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the EN1621 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the EN1621. The EN1621 contains a power down command to reduce power consumption.

Features

- Operating voltage: 2.4V~5.2V
- Built-in 256kHz RC oscillator
- 32x4 LCD driver
- External 33kHz crystal or 256kHz frequency source input
- Built-in 32x4 bit display RAM
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- 3-wire serial interface
- Internal time base frequency sources
- Internal LCD driving frequency source
- Two selectable buzzer frequency (2kHz/4kHz)
- Software configuration feature
- Data mode and command mode instructions
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage
- Power down command reduces power Consumption

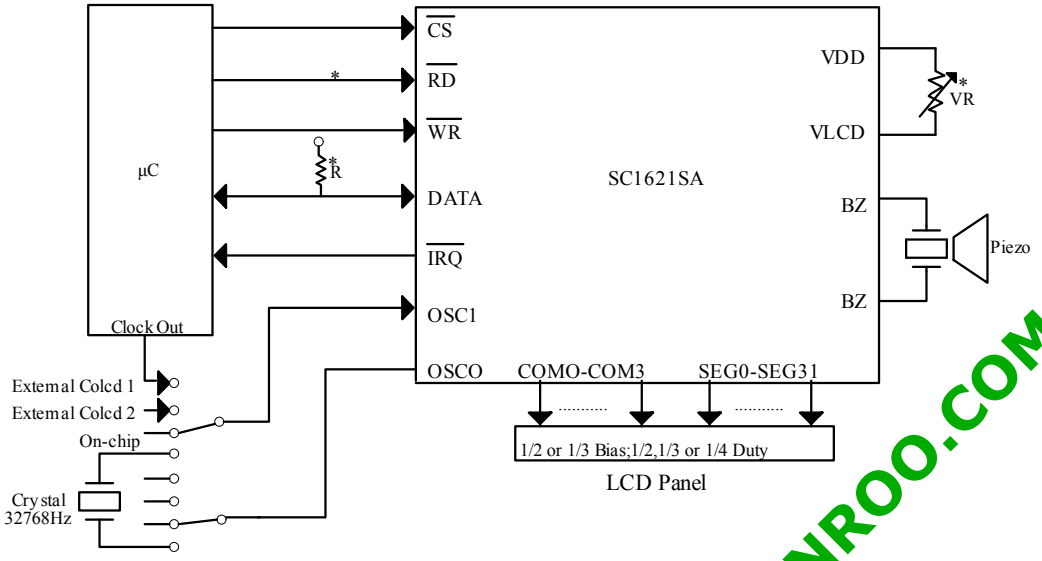
Block Diagram



The IC substrate should connected toVDD in the PCB layout artwork

Application Circuits

Host controller with an EN1621 display system



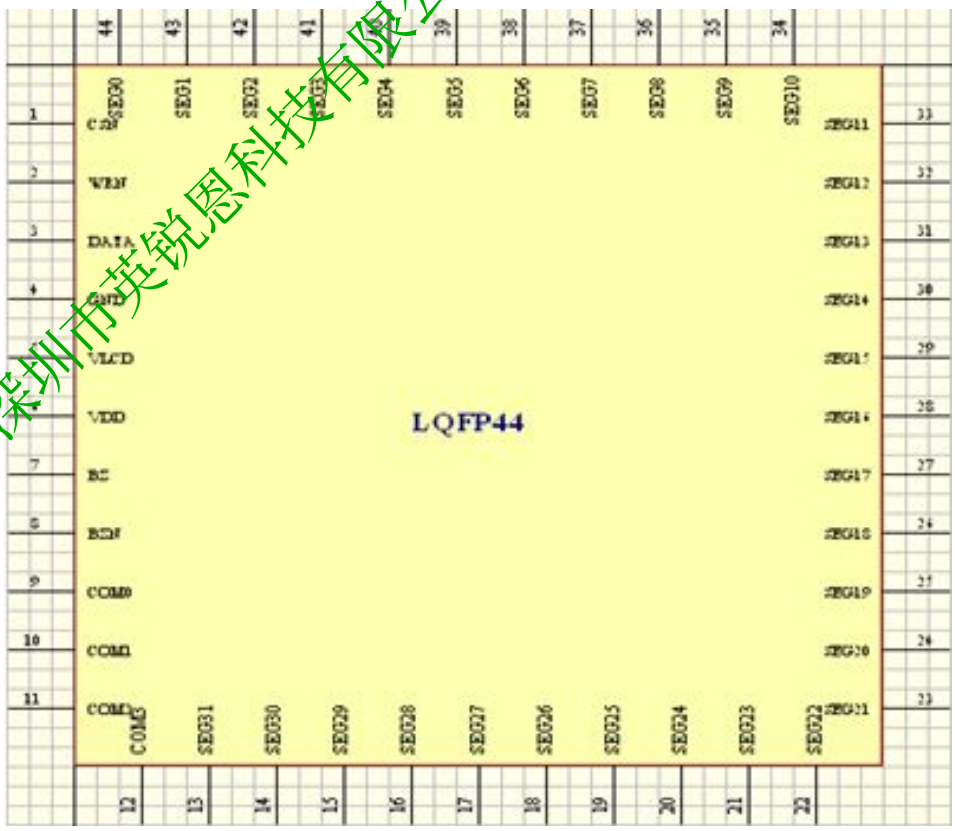
Note：The connection of IRQ and RD pin can sdldcted depending on the requirement of the µC.

The voltage applied to V_{LCD} pin must be lower than V_{DD}

Adjust VR to fit LCD display,at V_{DD} =5V, V_{LCD} =4V,VR=15k ±20%

Adjust R(external pull-high resistance)to fit user s time base clock.

PIN Description



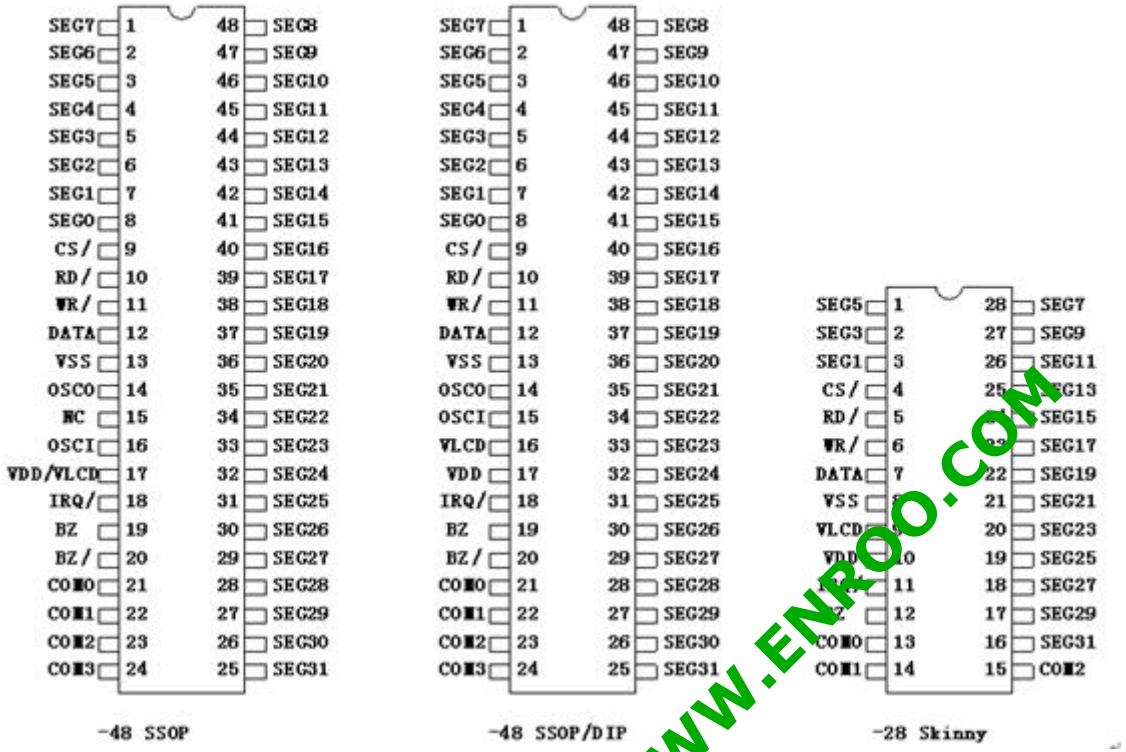
LQFP44:

NO.	PIN	NO.	PIN	NO.	PIN	NO.	PIN
1	CSN	**13**	SEG31	**25**	SEG19	**37**	SEG7
2	WRN	**14**	SEG30	**26**	SEG18	**38**	SEG6
3	DATA	**15**	SEG29	**27**	SEG17	**39**	SEG5
4	GND	**16**	SEG28	**28**	SEG16	**40**	SEG4
5	VLCD	**17**	SEG27	**29**	SEG15	**41**	SEG3
6	VDD	**18**	SEG26	**30**	SEG14	**42**	SEG2
7	BZ	**19**	SEG25	**31**	SEG13	**43**	SEG1
8	BZN	**20**	SEG24	**32**	SEG12	**44**	SEG0
9	COM0	**21**	SEG23	**33**	SEG11		
10	COM1	**22**	SEG22	**34**	SEG10		
11	COM2	**23**	SEG21	**35**	SEG9		
12	COM3	**24**	SEG20	**36**	SEG8		

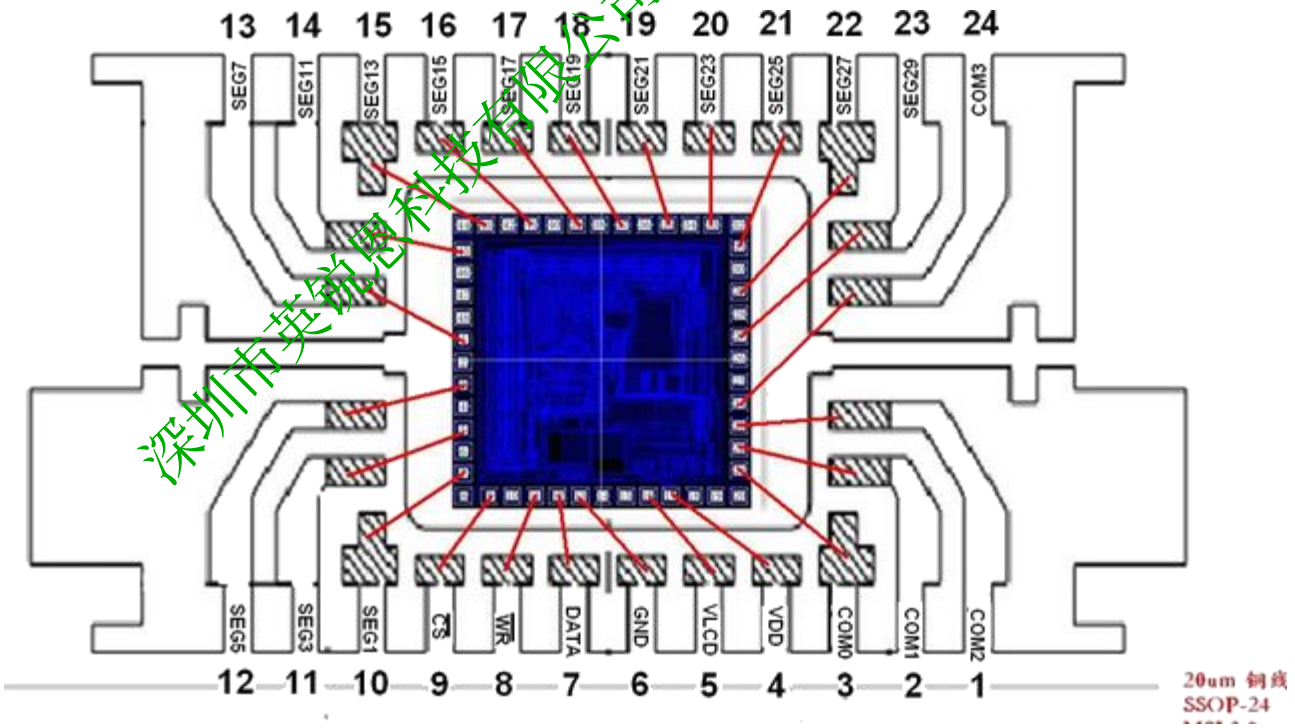
LQFP44:

Pad No.	Pad Name	I/O	Description
1	CSN	I	Chip selection input with pull-high resistor. When the CSN is logic high, the data and command read from or written to the EN1621 are disabled. The serial interface circuit is also reset. But if CSN is at logic low level and is input to the CSN pad, the data and command transmission between the host controller and the EN1621 are all enabled.
2	WRN	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the EN1621 onthe rising edge of the WRN signal.
3	DATA	I/O	Serial data input/output with pull-high resistor
4	GND	--	Negative power supply, ground
5	VLCD	I	VLCD I LCD power input
6	VDD	--	Positive power supply
7,8	BZ, BZN	O	2kHz or 4kHz tone frequency output pair
9~12	COM0~COM3	O	LCD common outputs
44~13	SEG0 ~ 31	O	LCD segment outputs

PIN Description



SSOP24 脚位图：



NO.	PIN	NO.	PIN	NO.	PIN	NO.	PIN
1	SEG7	**13**	VSS	**25**	SEG31	**37**	SEG19
2	SEG6	**14**	OSCO	**26**	SEG30	**38**	SEG18
3	SEG5	**15**	OSCI	**27**	SEG29	**39**	SEG17
4	SEG4	**16**	VLCD	**28**	SEG28	**40**	SEG16
5	SEG3	**17**	VDD	**29**	SEG27	**41**	SEG15
6	SEG2	**18**	IRQ/	**30**	SEG26	**42**	SEG14
7	SEG1	**19**	BZ	**31**	SEG25	**43**	SEG13
8	SEG0	**20**	BZ/	**32**	SEG24	**44**	SEG12
9	CS/	**21**	COM0	**33**	SEG23	**45**	SEG11
10	RD/	**22**	COM1	**34**	SEG22	**46**	SEG10
11	WR/	**23**	COM2	**35**	SEG21	**47**	SEG9
12	DATA	**24**	COM3	**36**	SEG20	**48**	SEG8

Pad No.	Pad Name	I/O	Description
1	CS-	I	Chip selection input with pull-high resistor. When the CS- is logic high, the data and command read from or written to the EN1621 are disabled. The serial interface circuit is also reset. But if CS- is at logic low level and is input to the CS- pad, the data and command transmission between the host controller and the EN1621 are all enabled.
2	RD-	I	READ clock input with pull-high resistor. Data in the RAM of the EN1621 are clocked out on the falling edge of the RD- signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	WR-	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the EN1621 on the rising edge of the WR-signal.
4	DATA	I/O	Serial data input/output with pull-high resistor
5	GND		Negative power supply, ground
6	OSCO	O	The OSCI and OSCO pads are connected to a 33kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if and on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
7	OSCI	I	
8	VLCD	I	VLCD I LCD power input
9	VDD	--	Positive power supply
10	IRQ	O	Time base or WDT overflow flag, NMOS open drain output
11,12	BZ, BZ-	O	2kHz or 4kHz tone frequency output pair
13~16	COM0~COM3	O	LCD common outputs
48~17	SEG0 ~ 31	O	LCD segment outputs

Absolute Maximum Ratings

Supply Voltage ---------- -0.3V ~ 5.5V
Input Voltage ---------- VSS - 0.3V ~ VDD + 0.3V
Storage Temperature ---------- -50℃ ~ 125℃
Operating Temperature ---------- -25℃~ 75℃

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute MRZCimum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Parameter	Sym	Min	Typ	MRZC	Units	Test Conditions	
						V_{DD}	Conditions
Operating Voltage	V_{DD}	2.4	--	5.2	V	--	
Stand by Current	I_{DD}	--	0.1	5.0	uA	3V	No load
		--	0.3	10		5V	Power down mode
Operating Current	I_{OP}	--	150	300	uA	3V	No load/LCD ON
		--	300	600		5V	On-chip RC oscillator
Operating Current	I_{OP}	--	60	120	uA	3V	No load/LCD ON
		--	120	240		5V	Crystal oscillator
Operating Current	I_{OP}	--	100	200	uA	3V	No load/LCD ON
		--	200	400		5V	External clock source
Input Low Voltage	V_{IL}	0	--	0.6	V	3V	DATA, WR-, CS-, RD-
		0	--	1.0		5V	
Input High Voltage	V_{IH}	2.4	--	3.0	V	3V	DATA, WR-, CS-, RD-
		4.0	--	5.0		5V	
DATA, BZ, BZN	I_{OL1}	0.5	1.2	--	mA	3V	V_{OL}=0.3V
		1.3	2.6	--		5V	V_{OL}=0.5V
DATA, BZ, BZN	I_{OH1}	-0.4	-0.8	--	mA	3V	V_{OH}=2.7V
		-0.9	-1.8	--		5V	V_{OH}=4.5 V
LCD Common Sink Current	I_{OL2}	80	150	--	uA	3V	V_{OL}=0.3V
		150	250	--		5V	V_{OL}=0.5V
LCD Common Source Current	I_{OH2}	-80	-120	--	uA	3V	V_{OH}=2.7V
		-120	-200	--		5V	V_{OH}=4.5 V
LCD Segment Sink Current	I_{OL3}	60	120	--	uA	3V	V_{OL}=0.3V
		120	200	--		5V	V_{OL}=0.5V
LCD Segment Source Current	I_{OH3}	-40	-70	--	uA	3V	V_{OH}=2.7V
		-70	-100	--		5V	V_{OH}=4.5 V
Pull High Resistor	R_{PH}	40	80	150	KΩ	3V	DATA, WR-, CS-

		30	60	100		5V	

A.C. Characteristics

Parameter	Sym	Min	Typ	MRZC	Units	Test Conditions	
						V_{DD}	Conditions
System Clock	f_{SYS1}	--	256	--	KHz	3V	On Chip RC Oscillator
		--	256	--		5V	
System Clock	f_{SYS2}		33		KHz	3V	Crystal Oscillator
			33			5V	
System Clock	f_{SYS3}		256		KHz	3V	External clock source
			256			5V	
LCD Clock	f_{LCD}	--	$F_{SYS1}/1024$	--	Hz	--	On-chip RC oscillator
		--	$F_{SYS2}/128$	--			Crystal Oscillator
		--	$F_{SYS3}/1024$	--			External clock source
LCD Common Period	t_{COM}	--	n/f_{LCD}	--	S		n: Number of COM
Serial Date Clock (WRN Pin)	f_{CLK1}	--	--	150	KHz	3V	Duty cycle 50%
		--	--	300		5V	
		--	--	150		5V	
Tone Frequency	f_{TONE}	--	2.0 or 4.0	--	KHz	--	On-chip RC oscillator
Serial Interface Reset Pulse Width (Figure 3)	t_{CS}	--	250		ns	3V	CS-
						5V	
WRN Input Pulse Width (Figure 1)	t_{CLK}	3.34	--	--	us	3V	Write mode
		6.67	--	--		5V	Read mode
		1.67	--	--		3V	Write mode
		3.34	--	--		5V	Read mode
Rise/Full Time Serial Data Clock Width (Figure 1)	$t_r t_f$	--	120	--	ns	3V	
						5V	
Setup Time for Data to WRN, Clock Width (Figure 1)	t_{su}	--	120	--	ns	3V	
						5V	
Hold Time for Data to WRN Clock Width (Figure 1)	t_h	--	120	--	ns	3V	
						5V	
Setup Time for Data to CSN Clock Width (Figure 1)	t_{su1}	--	100	--	ns	3V	
						5V	
Hold Time for Data to CSN Clock Width (Figure 1)	t_{h1}	--	100	--	ns	3V	
						5V	

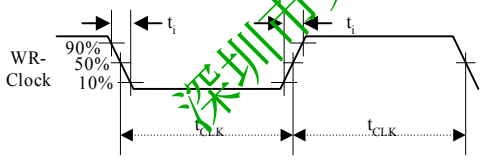


Figure 1

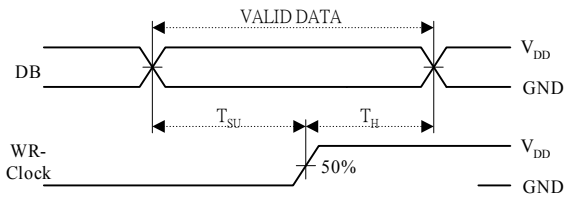


Figure 2

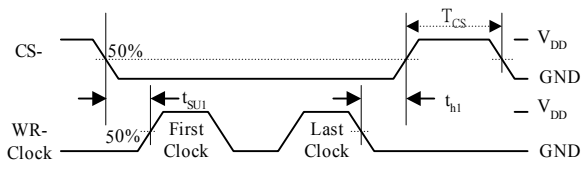
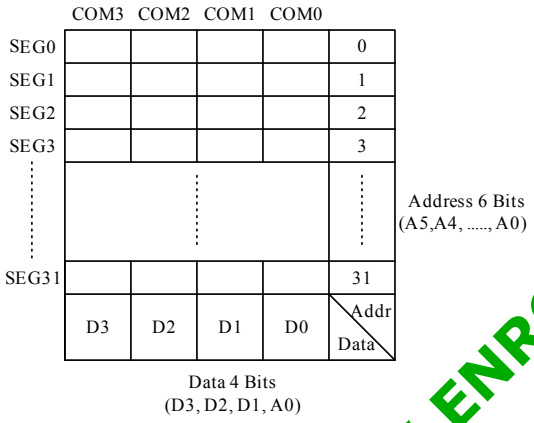


Figure 3

Functional Description

- **Display memory – RAM**

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:

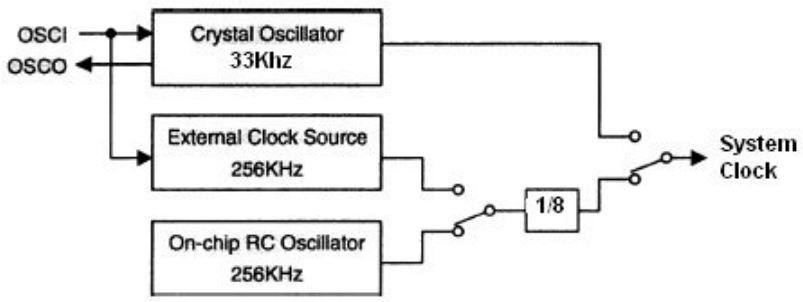


RAM Mapping

- **System oscillator**

The EN1621 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256 kHz), a crystal oscillator (33 kHz), or an external 256 kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

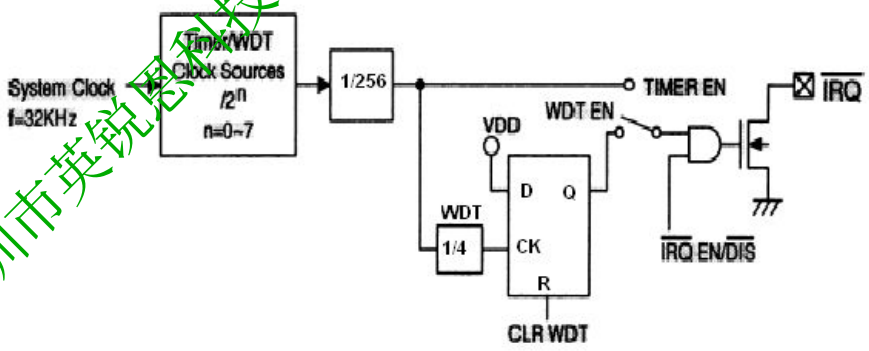
The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 33 kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256 kHz clock source operation. At the initial system power on, the EN1621 is at the SYS DIS state.



- **Time base and Watchdog Timer (WDT)**

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate

time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the IRQ- output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation. $f_{WDT}=\frac{32kHz}{2^n}$ where the value of n ranges from 0 to 7 by command options. The 33 kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 33 kHz, an on-chip oscillator (256 kHz), or an external frequency of 256 kHz. If an on-chip oscillator (256 kHz) or an external 256 kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 33 kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator where as executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the IRQ- pin). After the TIMER EN command is transferred, the WDT is disconnected from the IRQ- pin, and the output of the time base generator is connected to the IRQ- pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the IRQ- EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the IRQ- pin will stay at a logic low level until the CLR WDT or the IRQ- DIS command is issued. After the IRQ- output is disabled the IRQ- pin will remain at the floating state. The IRQ- output can be enabled or disabled by executing the IRQ- EN or the IRQ- DIS command, respectively. The IRQ- EN makes the output of the time base generator or of the WDT time-out flag appear on the IRQ- pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.



On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the EN1621 will continue working until system power fails or the external clock source is removed. After the system power on, the IRQ- will be disabled.

- **Tone output**

A simple tone generator is implemented in the EN1621. The tone generator can output a pair of differential driving signals on the BZ and BZ-, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone

frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and BZ-, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the BZ- outputs will remain at low level.

- **LCD Driver**

The EN1621 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the EN1621 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 33kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 100, namely 100, indicates the command mode ID. If successive commands have been

Name	Command Code	Function
LCD OFF	1 0 0 0 0 0 0 0 0 1 0 X	Turn off LCD output
LCD ON	1 0 0 0 0 0 0 0 0 1 1 X	Turn on LCD output
BIAS&COM	1 0 0 0 0 1 0 a b X c X	c=0:1/2 bias option
		c=1:1/3 bias option
		ab=00:2 commons option
		ab=01:3 commons option
		ab=10:4 commons option

issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the EN1621 can be compatible with most types of LCD panels.

- **Commanded Formant**

The EN1621 can be configured by the S/W setting. There are two mode commands to configure the EN1621 resources and to transfer the LCD display data. The configuration mode of the EN1621 is called command mode, and its command mode ID is 100. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 100, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CS- pin should be set to “1” and the previous operation mode will be reset also. Once the CS- pin returns to “0” a new operation mode ID should be issued first.

- **Interfacing**

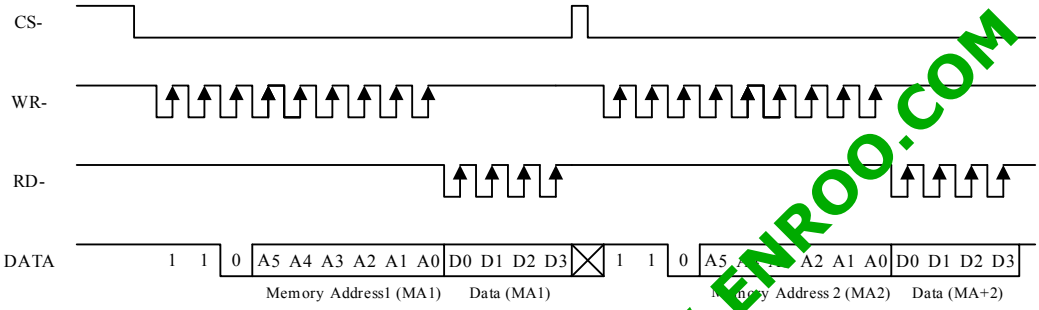
Only four lines are required to interface with the EN1621. The CS- line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the EN1621. If the CS- pin is set to 1, the data and command issued between the host controller and the EN1621 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the EN1621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The RD- line is the READ clock input. Data in the RAM are clocked out on the falling

edge of the RD- signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between

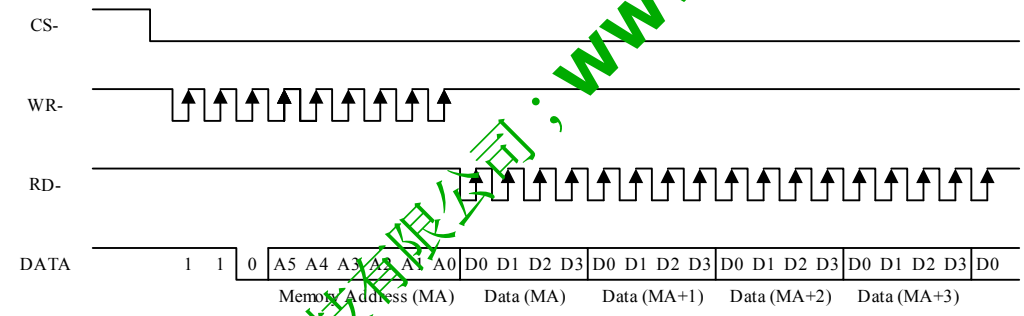
The rising edge and the next falling edge of the RD- signal. The WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the EN1621 on the rising edge of the WR signal. There is an optional IRQ- line to be used as an interface between the host controller and the EN1621. The IRQ- pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the IRQ- pin of the EN1621.

Timing Diagrams

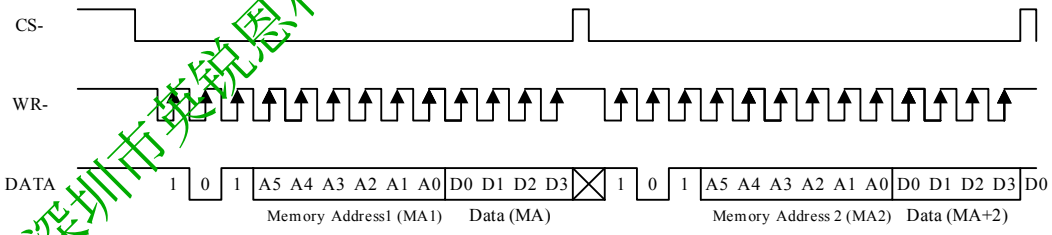
- READ mode (commanded code: 110)



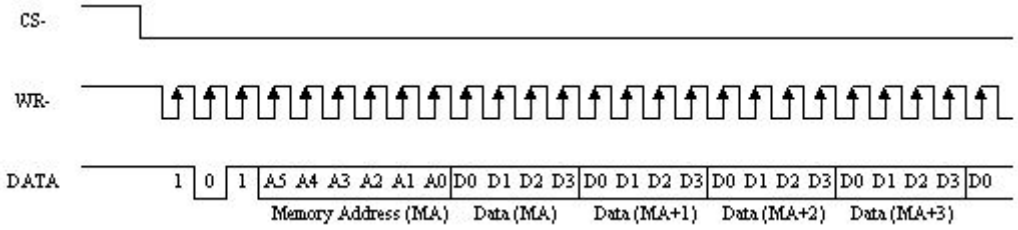
- READ mode (successive address reading)



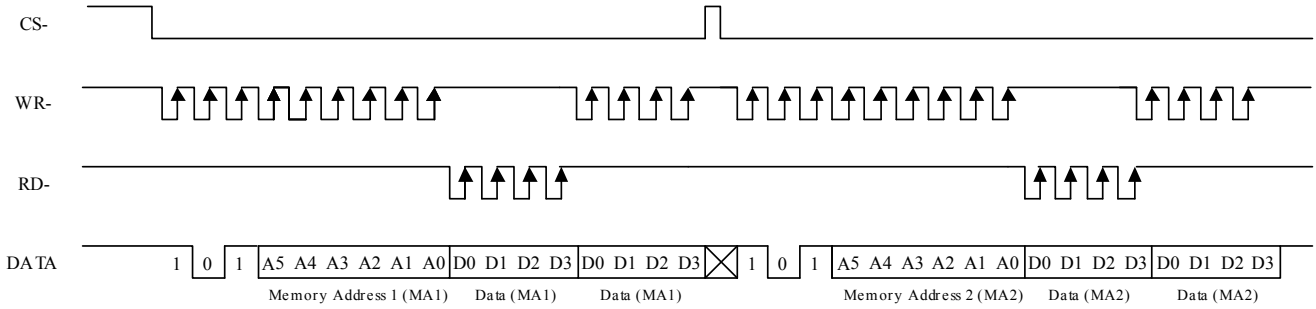
- WRITE mode (command code: 1 0 1)



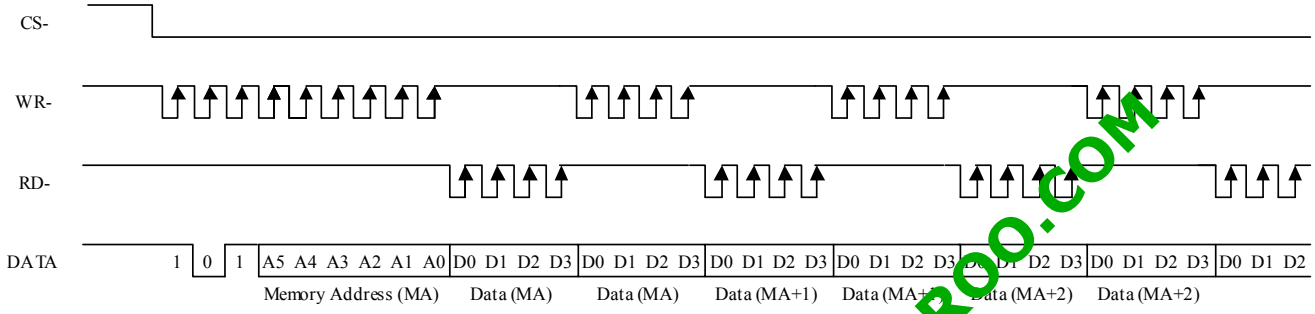
- WRITE mode (successive address writing)



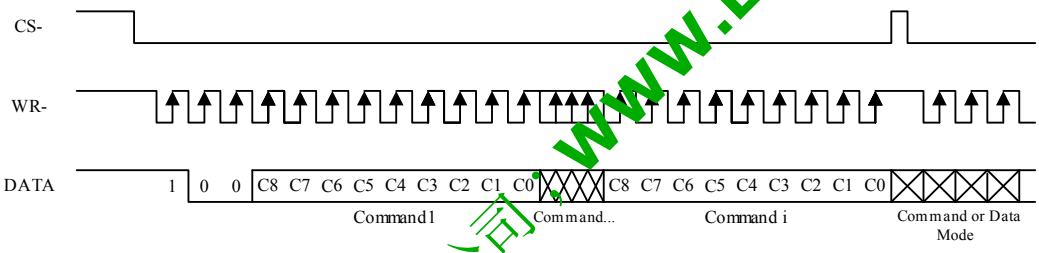
- READ-MODIFY-WRITE mode (command code: 1 0 1)



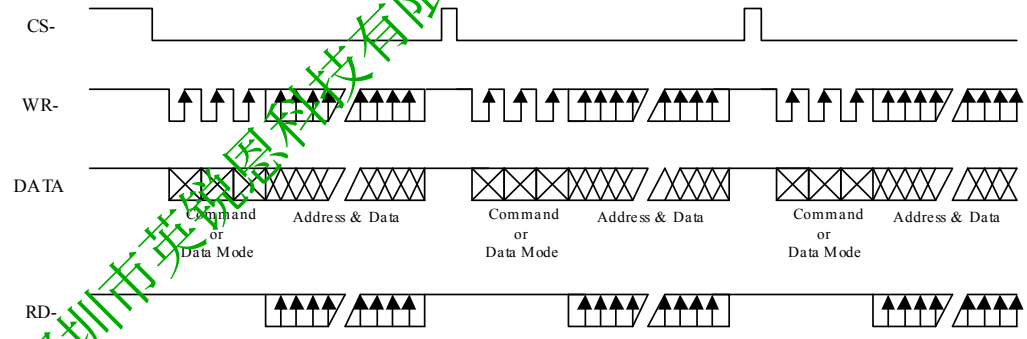
➢ READ-MODIFY-WRITE mode (successive address accessing)



➢ Command mode (command code: 100)



➢ Mode (data and command mode)



Note:

It is recommended that the host controller should read in the data from the DATA line between the rising edge of the RD- line and the falling edge of the next RD- line.

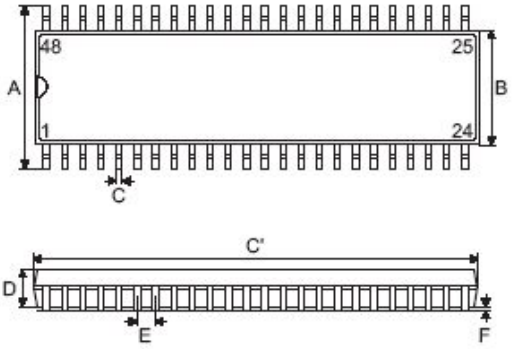
Command Summary

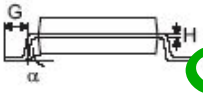
Name	ID	Command Code	D/C	Function	Def.
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010X	C	Turn off LCD bias generator	Yes
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	100	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
XTAL32K	100	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	100	001-10XX-X	C	System clock source, external clock source	Yes
EXT 256K	100	0001-11XX-X	C	System clock source, external clock	
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2 bias option ab=00:2 command option ab=01:3 commons option ab=10:4 commons option	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00:2 command option ab=01:3 commons option ab=10:4 commons option	
TONE 4K	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	100	011X-XXXX-X	C	Tone frequency, 2kHz	
F1	100	101X-X000-X	C	Time base/WDT clock; output: 1Hz; The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output: 2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output: 4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	100	1110-0000-X	C		
NORMAL	100	1110-0011-X	C		Yes

Package Information

Package Information

48-pin SSOP (300mil) Outline Dimensions





Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	395	—	420
B	291	—	299
C	8	—	12
C'	613	—	637
D	85	—	99
E	—	25	—
F	4	—	10
G	25	—	35
H	—	—	12
α	0°	—	8°

ENROO 英锐恩

单片机集成方案全方位解决服务商

优质智能电子产品“芯”方案解决商

联系信息：

深圳市英锐恩科技有限公司
ENROO-TECH（SHENZHEN）CO.,LTD
中国·深圳市福田区福华路嘉汇新城汇商中心27楼2701室

Enroo-Tech Technologies CO., Limited
香港荃灣青山道 388 號中國染廠大厦 17 樓 A 室

联系电话：86-755-82543411,83167411,83283911,88845951
联系传真：86-755-82543511
全国热线：4007-888-234
联系邮件：enroo@enroo.com
公司网站：http://www.enroo.com http://www.enroo-tech.com